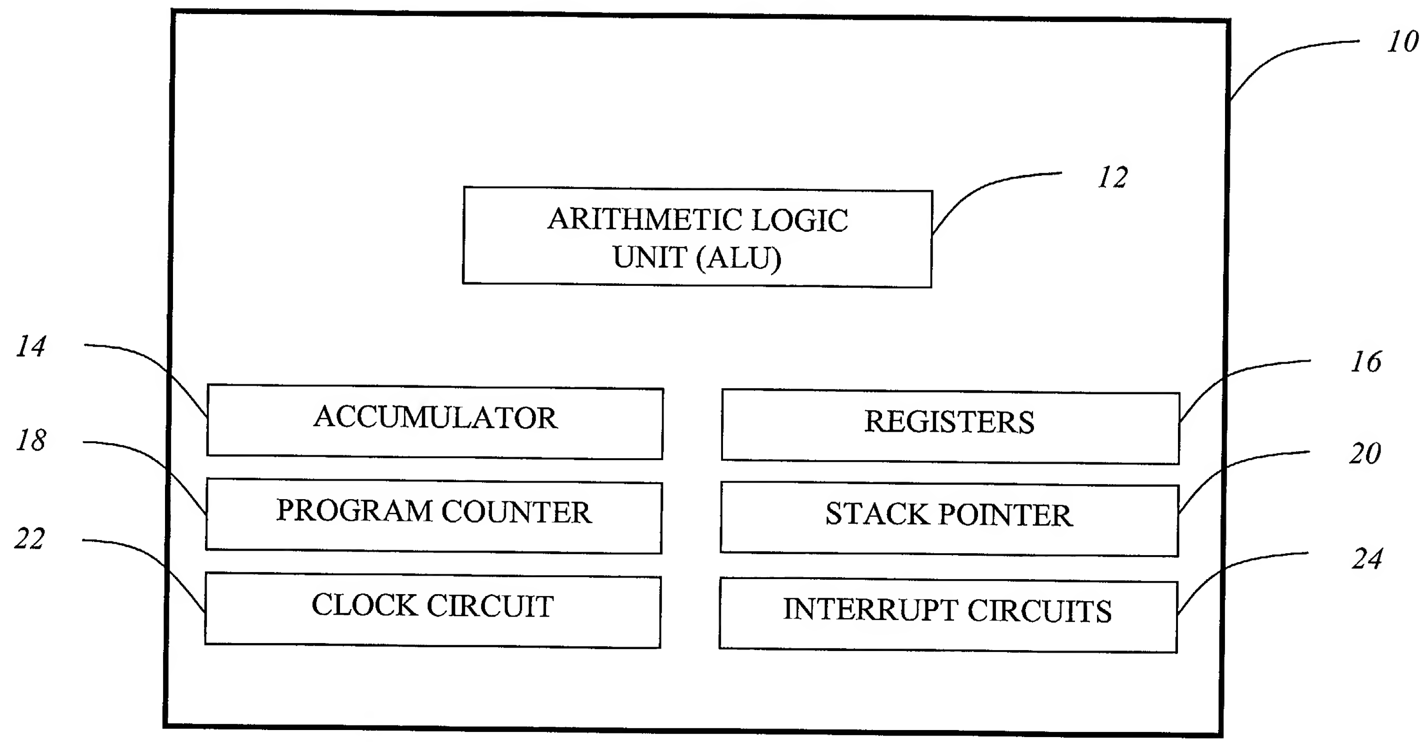
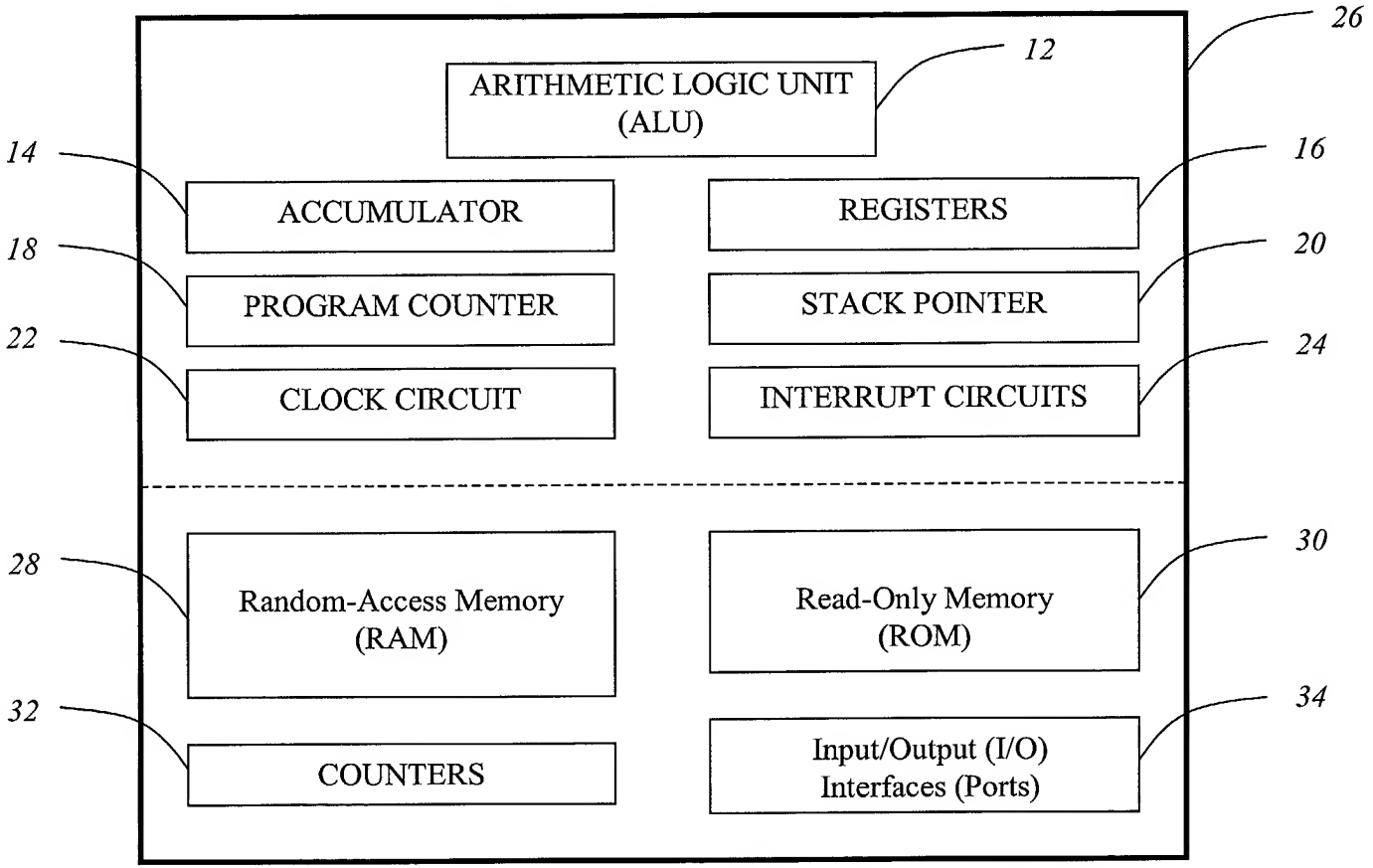


Prior Art

Figure 1



Prior Art

Figure 2

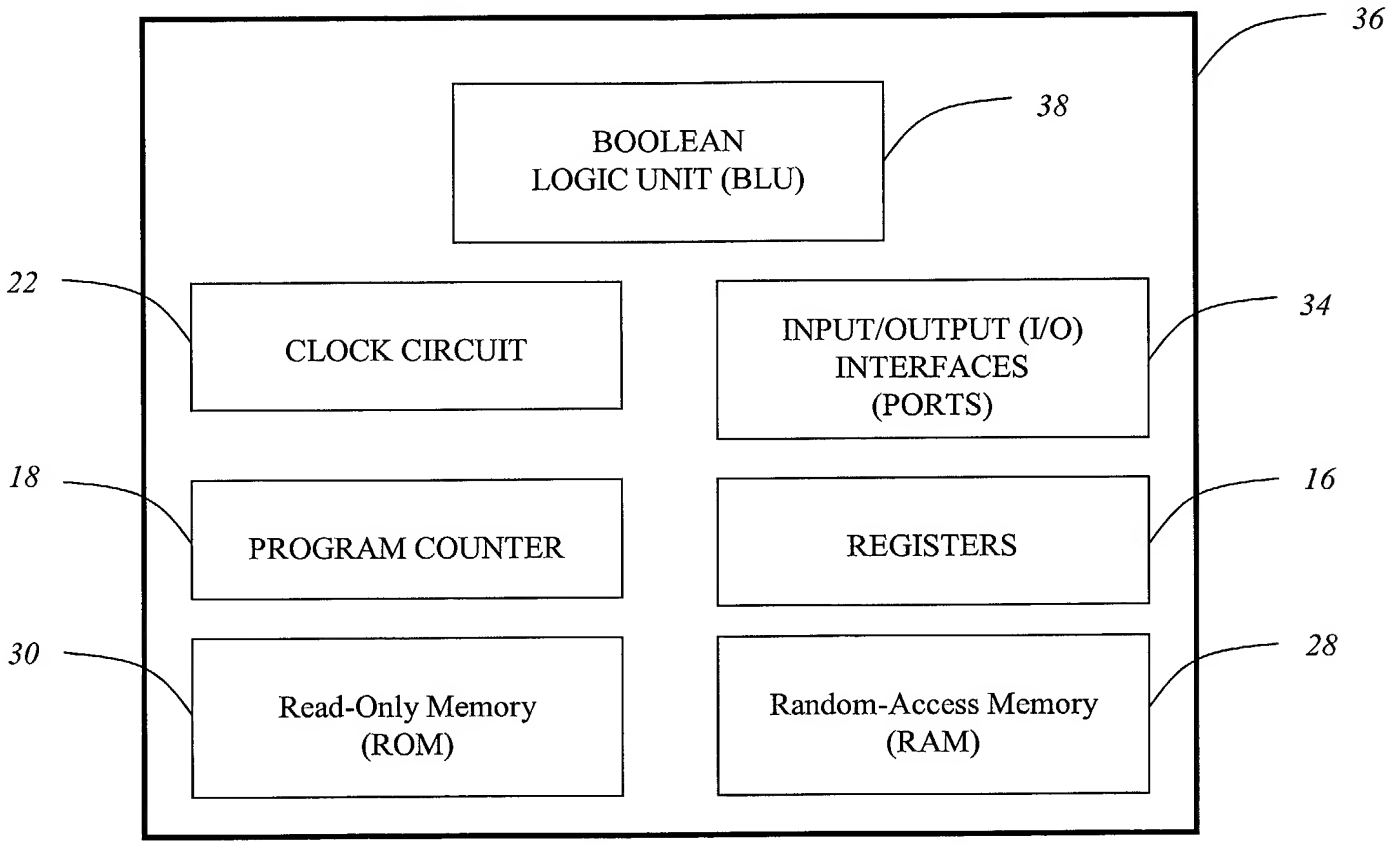


Figure 3

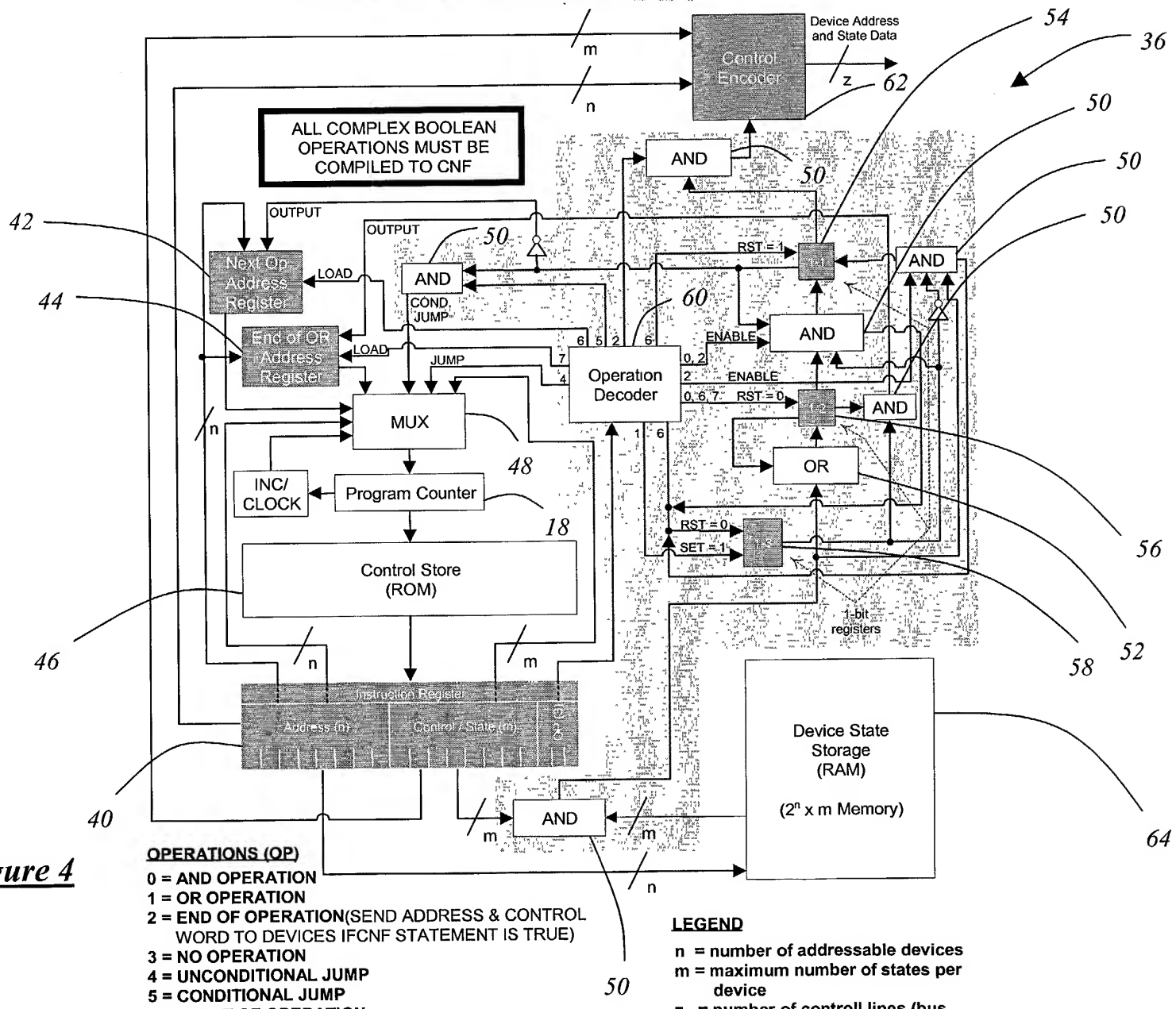


Figure 4

OPERATIONS (OP)

0 = AND OPERATION
1 = OR OPERATION
2 = END OF OPERATION(SEND ADDRESS & CONTROL WORD TO DEVICES IFCNF STATEMENT IS TRUE)
3 = NO OPERATION
4 = UNCONDITIONAL JUMP
5 = CONDITIONAL JUMP
6 = START OF OPERATION
7 = START OF OR CONJUNCT

LEGEND

n = number of addressable devices
m = maximum number of states per device
z = number of controll lines (bus size/width)

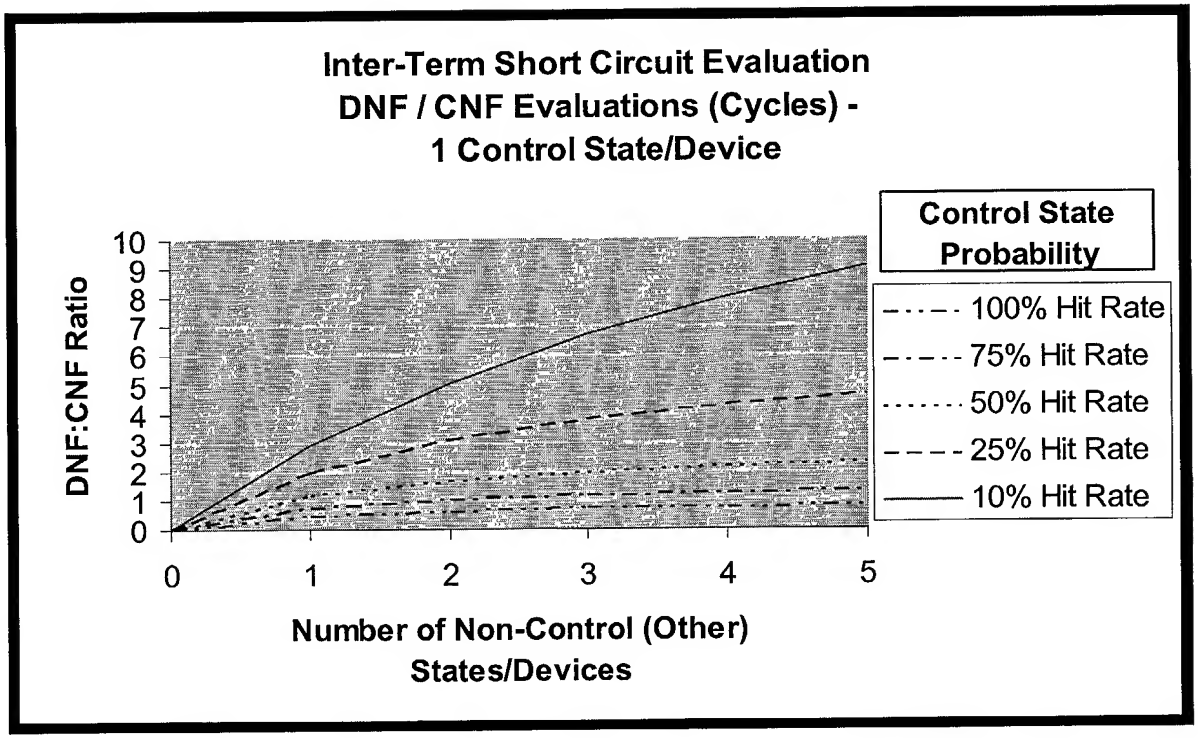


Figure 5

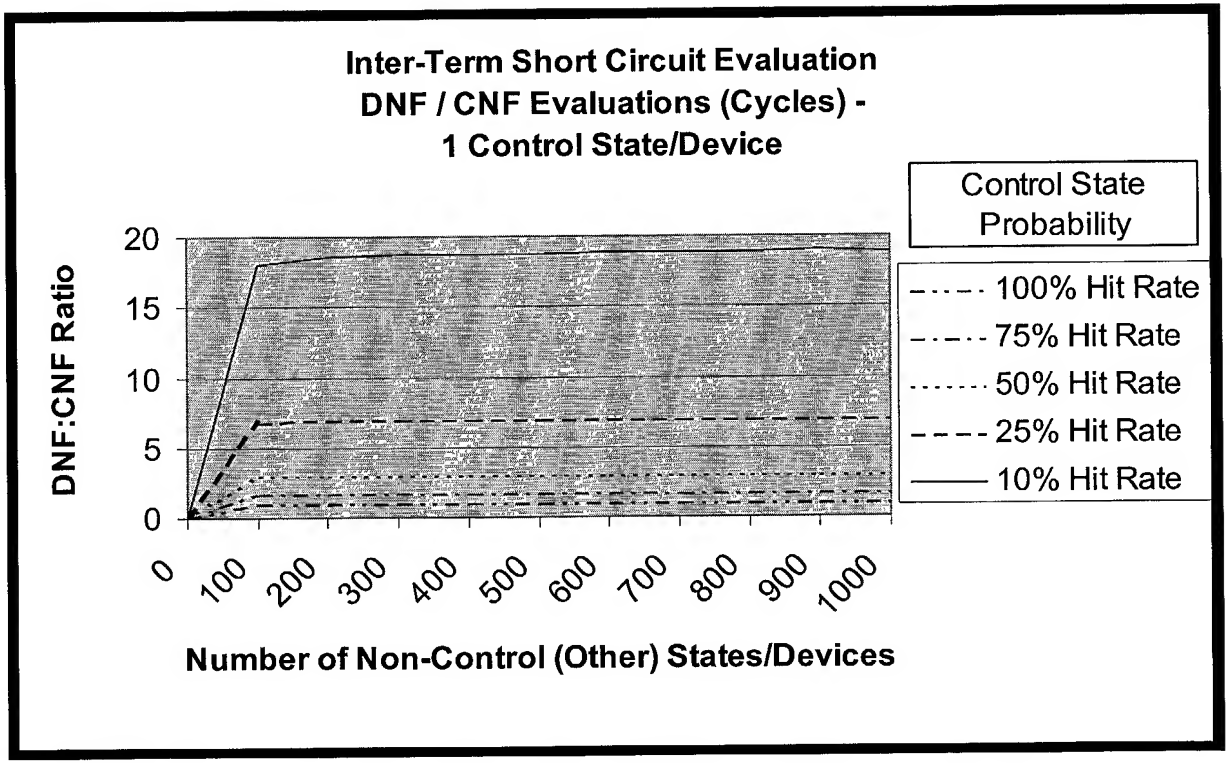

Inter-Term Short Circuit Evaluation
DNF / CNF Evaluations (Cycles) -
1 Control State/Device
DNF:CNF Ratio
20
15
10
5
0
0
100
200
300
400
500
600
700
800
900
1000
Number of Non-Control (Other) States/Devices
Control State Probability
100% Hit Rate
75% Hit Rate
50% Hit Rate
25% Hit Rate
10% Hit Rate

Figure 6

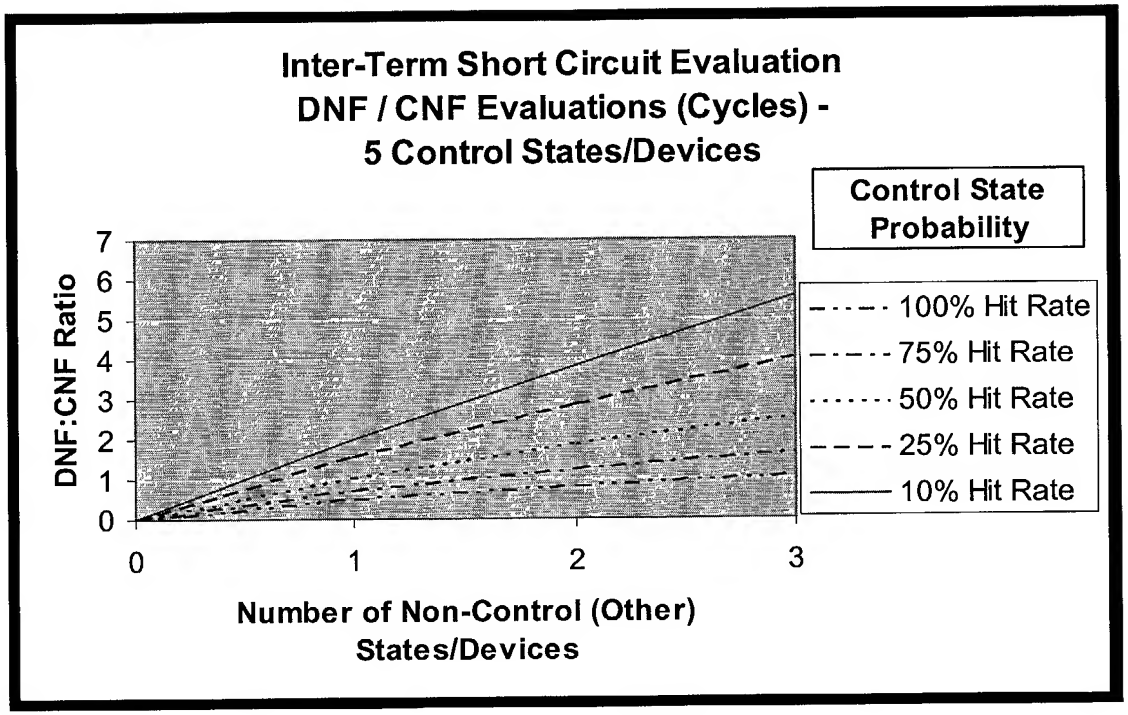


Figure 7

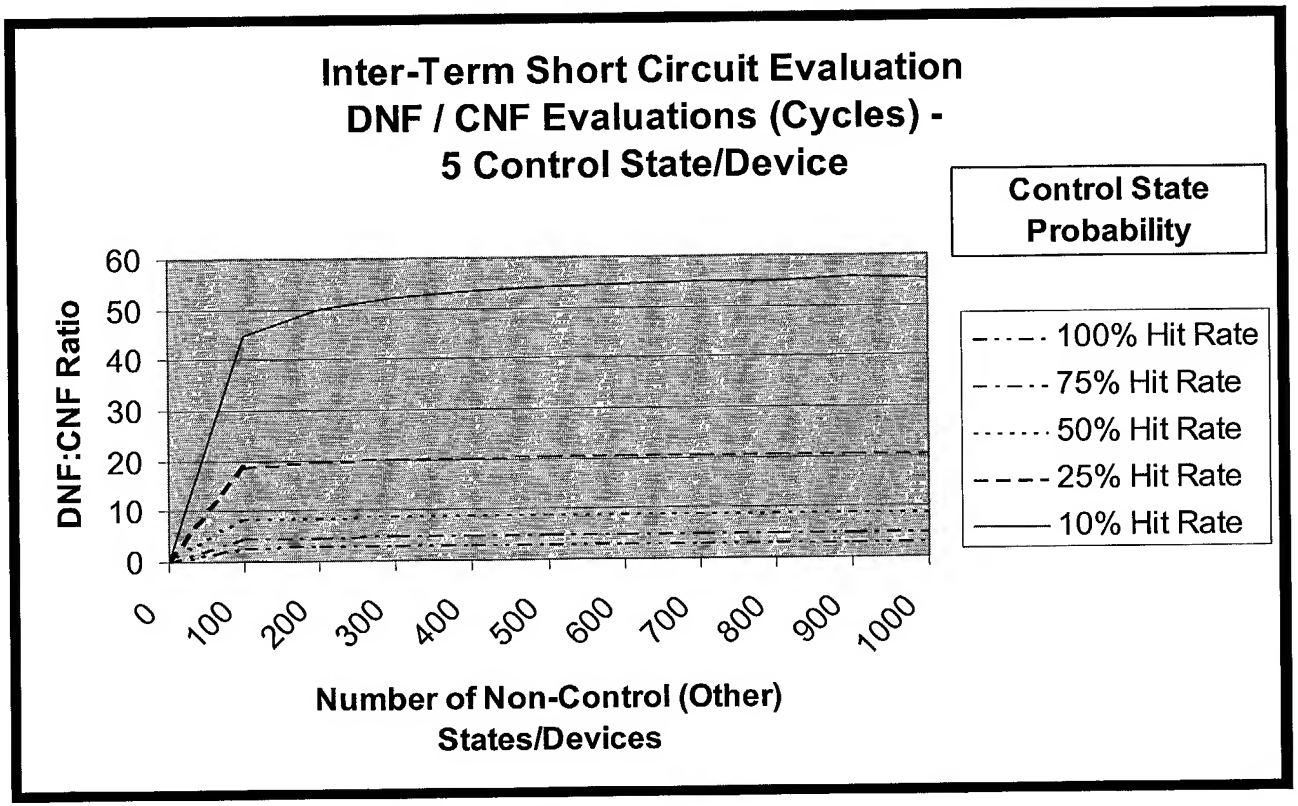

Inter-Term Short Circuit Evaluation
DNF / CNF Evaluations (Cycles) -
5 Control State/Device
DNF:CNF Ratio
60
50
40
30
20
10
0
0
100
200
300
400
500
600
700
800
900
1000
Number of Non-Control (Other)
States/Devices
Control State
Probability
100% Hit Rate
75% Hit Rate
50% Hit Rate
25% Hit Rate
10% Hit Rate

Figure 8

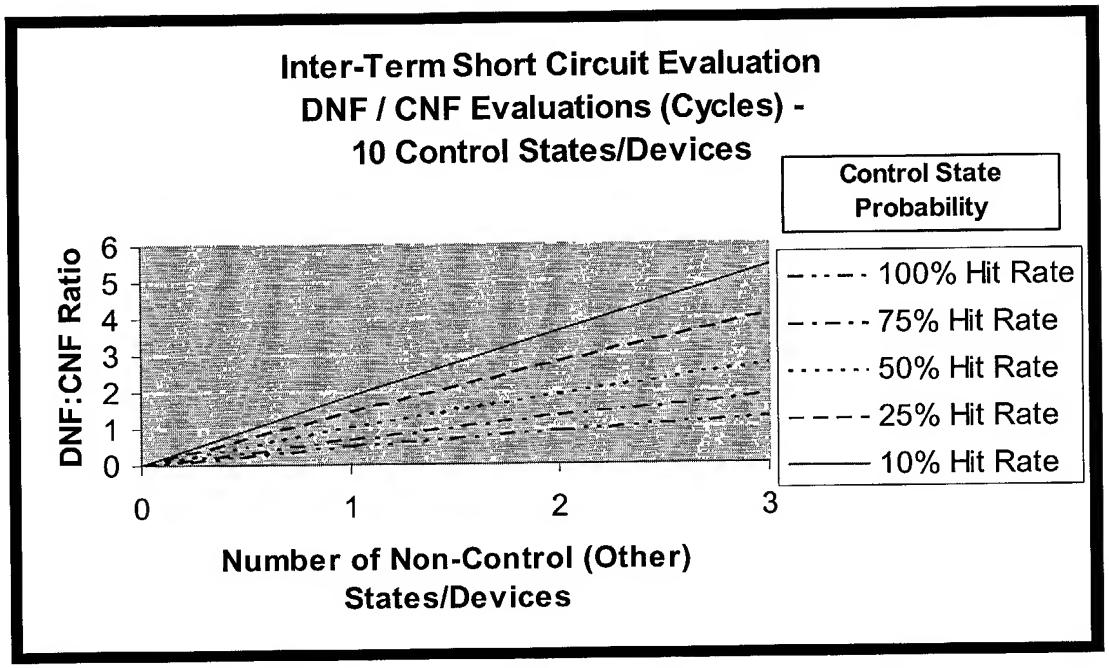

Inter-Term Short Circuit Evaluation
DNF / CNF Evaluations (Cycles) -
10 Control States/Devices
Control State Probability
100% Hit Rate
75% Hit Rate
50% Hit Rate
25% Hit Rate
10% Hit Rate
DNF:CNF Ratio
0
1
2
3
4
5
6
0
1
2
3
Number of Non-Control (Other) States/Devices

Figure 9

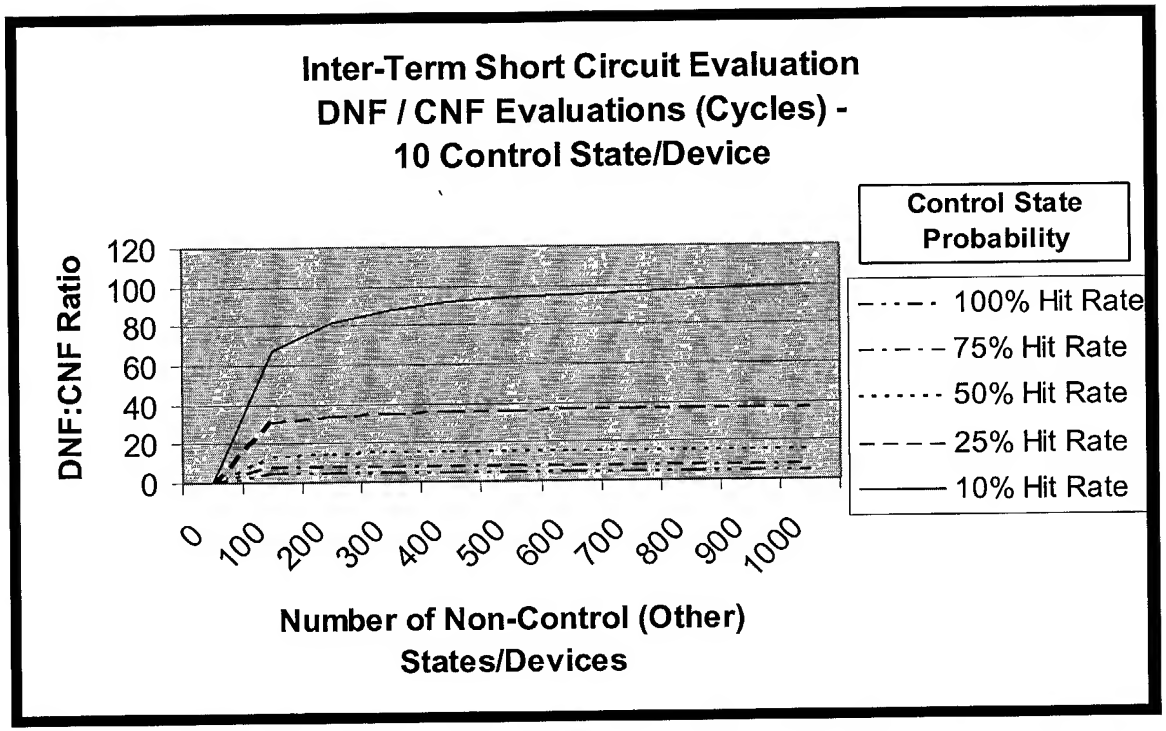

Inter-Term Short Circuit Evaluation
DNF / CNF Evaluations (Cycles) -
10 Control State/Device
DNF:CNF Ratio
120
100
80
60
40
20
0
0
100
200
300
400
500
600
700
800
900
1000
Number of Non-Control (Other)
States/Devices
Control State
Probability
100% Hit Rate
75% Hit Rate
50% Hit Rate
25% Hit Rate
10% Hit Rate

Figure 10

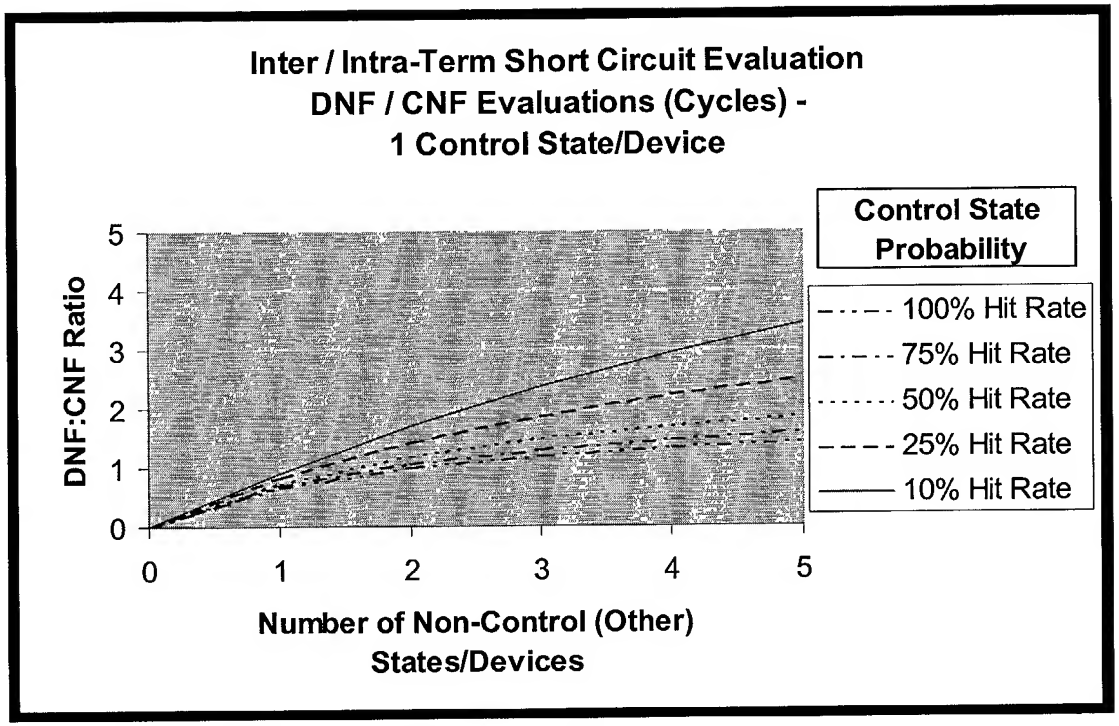

Inter / Intra-Term Short Circuit Evaluation
DNF / CNF Evaluations (Cycles) -
1 Control State/Device
DNF:CNF Ratio
0
1
2
3
4
5
Number of Non-Control (Other) States/Devices
Control State Probability
100% Hit Rate
75% Hit Rate
50% Hit Rate
25% Hit Rate
10% Hit Rate

Figure 11

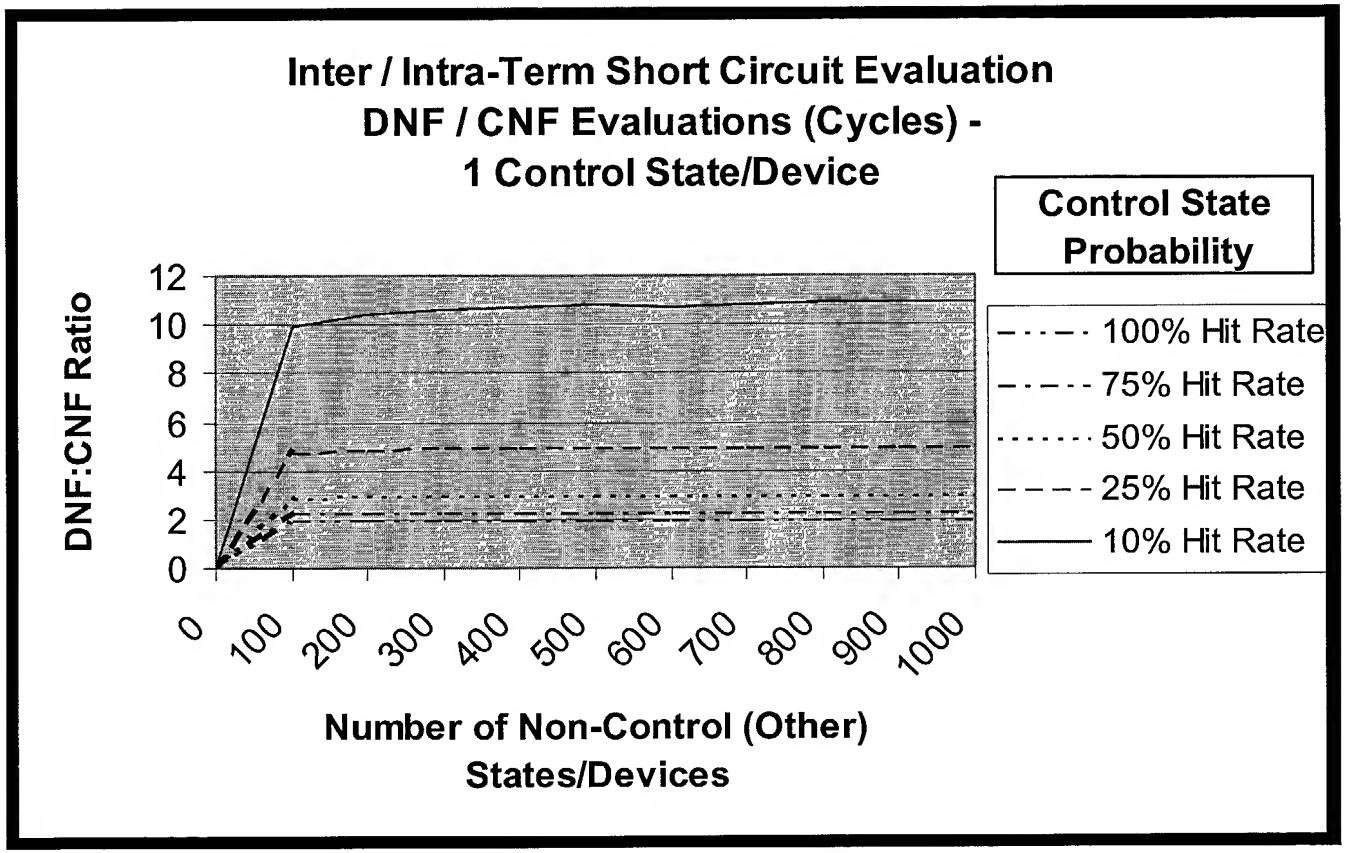

Inter / Intra-Term Short Circuit Evaluation
DNF / CNF Evaluations (Cycles) -
1 Control State/Device
DNF:CNF Ratio
12
10
8
6
4
2
0
0
100
200
300
400
500
600
700
800
900
1000
Number of Non-Control (Other)
States/Devices
Control State
Probability
100% Hit Rate
75% Hit Rate
50% Hit Rate
25% Hit Rate
10% Hit Rate

Figure 12

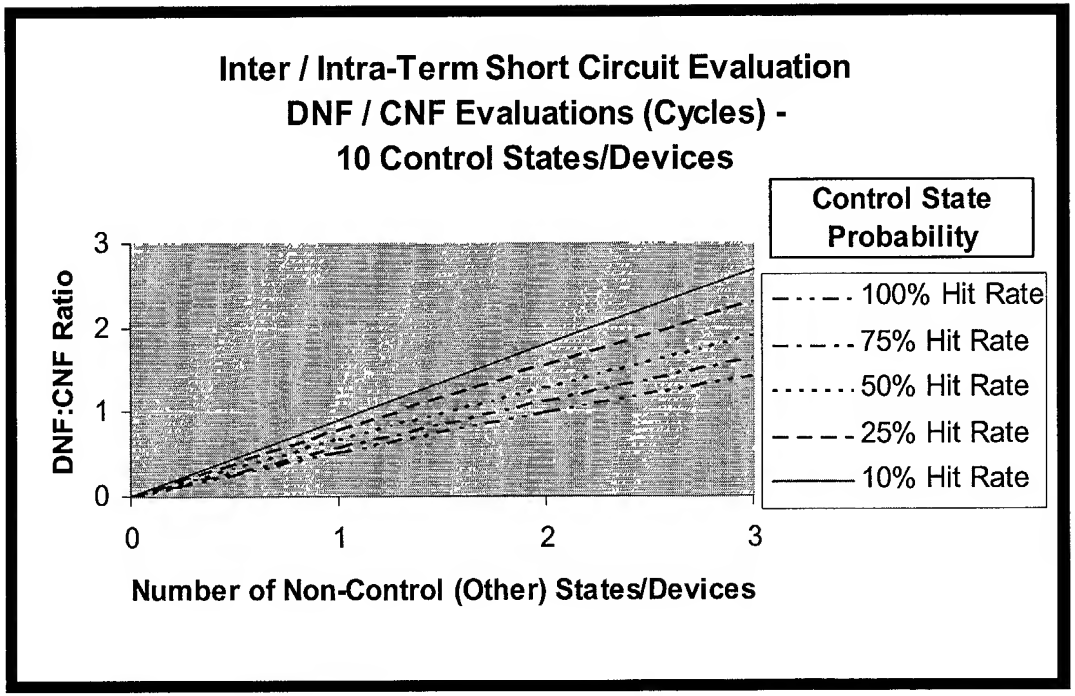

Inter / Intra-Term Short Circuit Evaluation
DNF / CNF Evaluations (Cycles) -
10 Control States/Devices
Control State Probability
100% Hit Rate
75% Hit Rate
50% Hit Rate
25% Hit Rate
10% Hit Rate
DNF:CNF Ratio
0
1
2
3
Number of Non-Control (Other) States/Devices

Figure 13

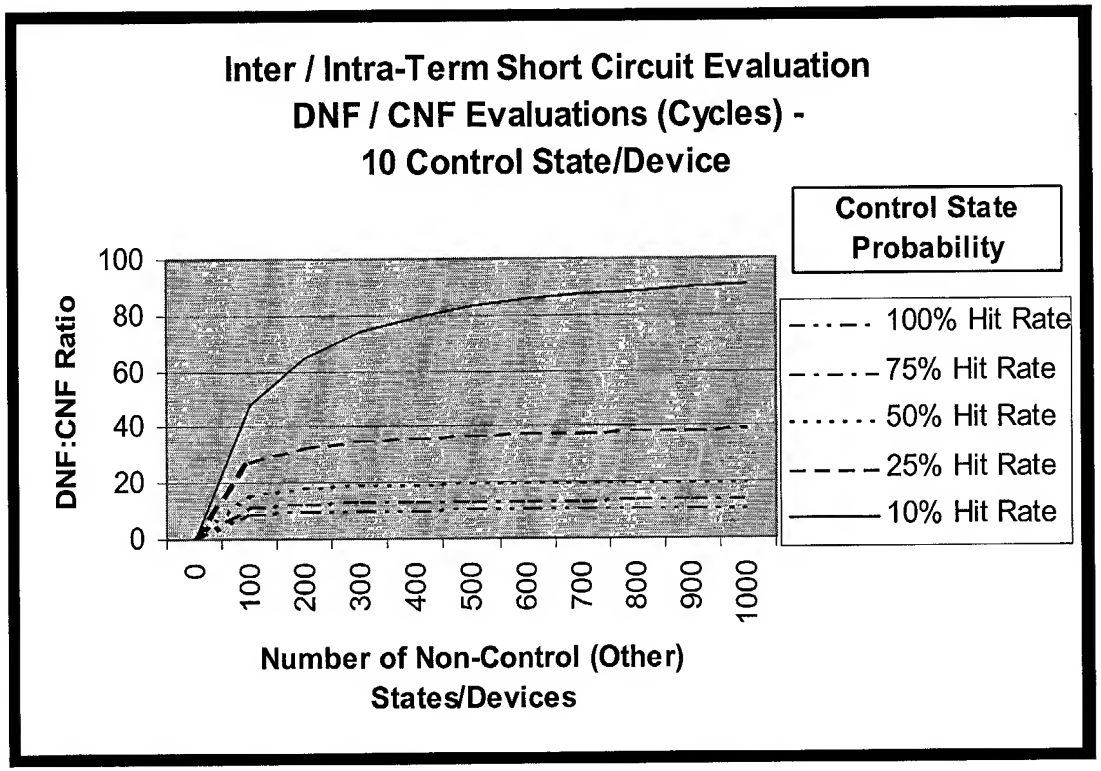

Inter / Intra-Term Short Circuit Evaluation
DNF / CNF Evaluations (Cycles) -
10 Control State/Device
Control State Probability
100% Hit Rate
75% Hit Rate
50% Hit Rate
25% Hit Rate
10% Hit Rate
DNF:CNF Ratio
100
80
60
40
20
0
0
100
200
300
400
500
600
700
800
900
1000
Number of Non-Control (Other) States/Devices

Figure 14

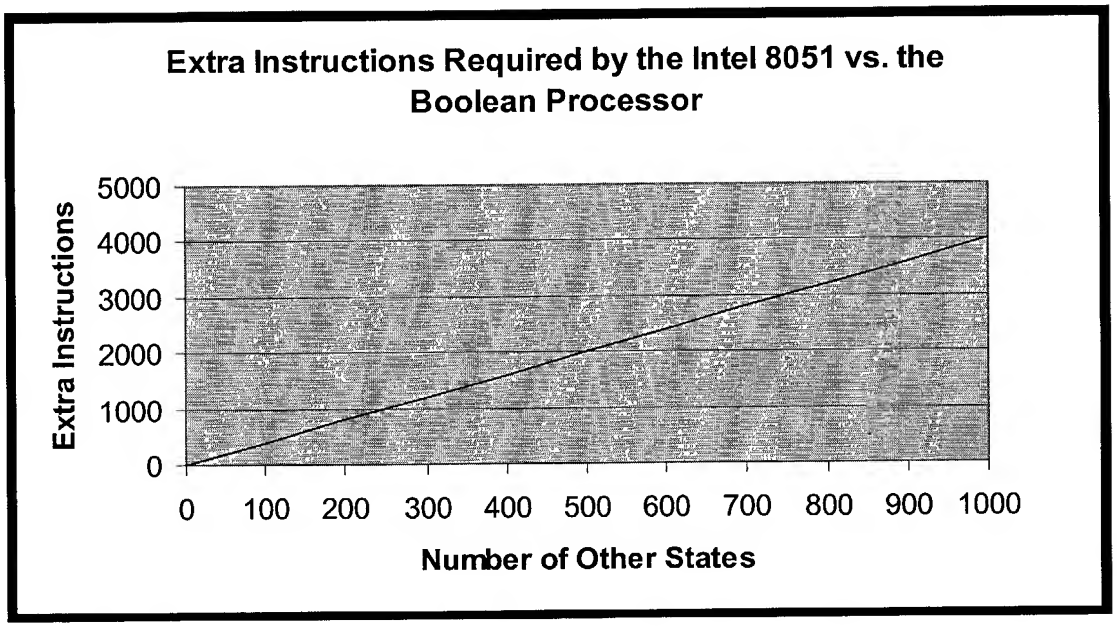

Extra Instructions Required by the Intel 8051 vs. the Boolean Processor
Extra Instructions
5000
4000
3000
2000
1000
0
0
100
200
300
400
500
600
700
800
900
1000
Number of Other States

Figure 15

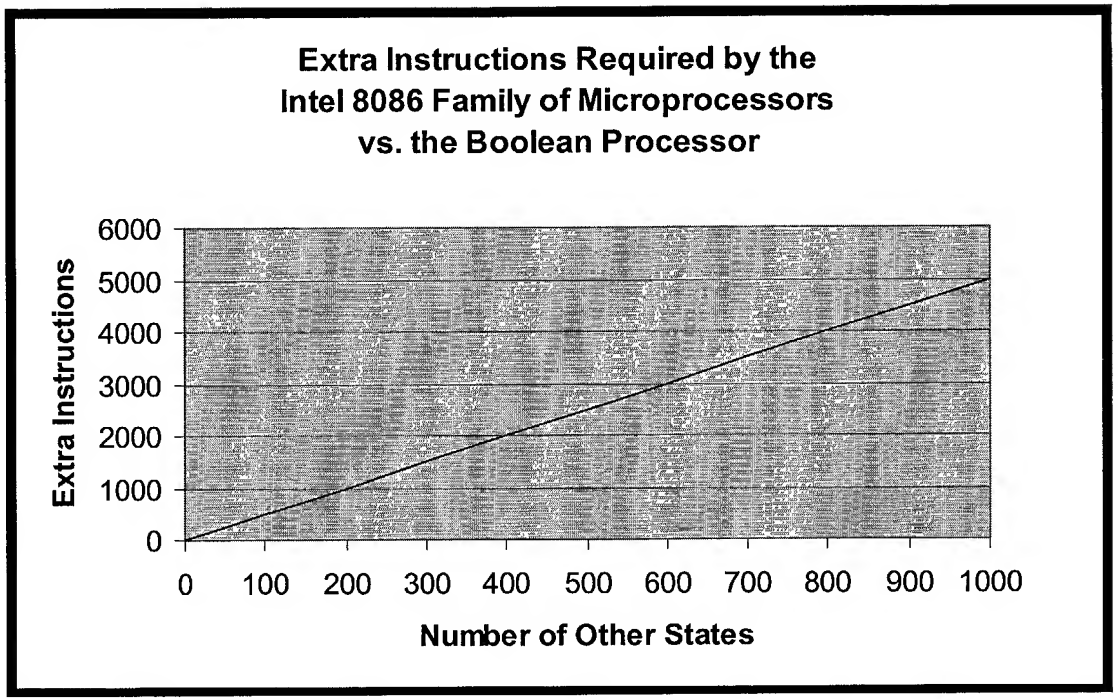

Extra Instructions Required by the
Intel 8086 Family of Microprocessors
vs. the Boolean Processor
Extra Instructions
6000
5000
4000
3000
2000
1000
0
0
100
200
300
400
500
600
700
800
900
1000
Number of Other States

Figure 16

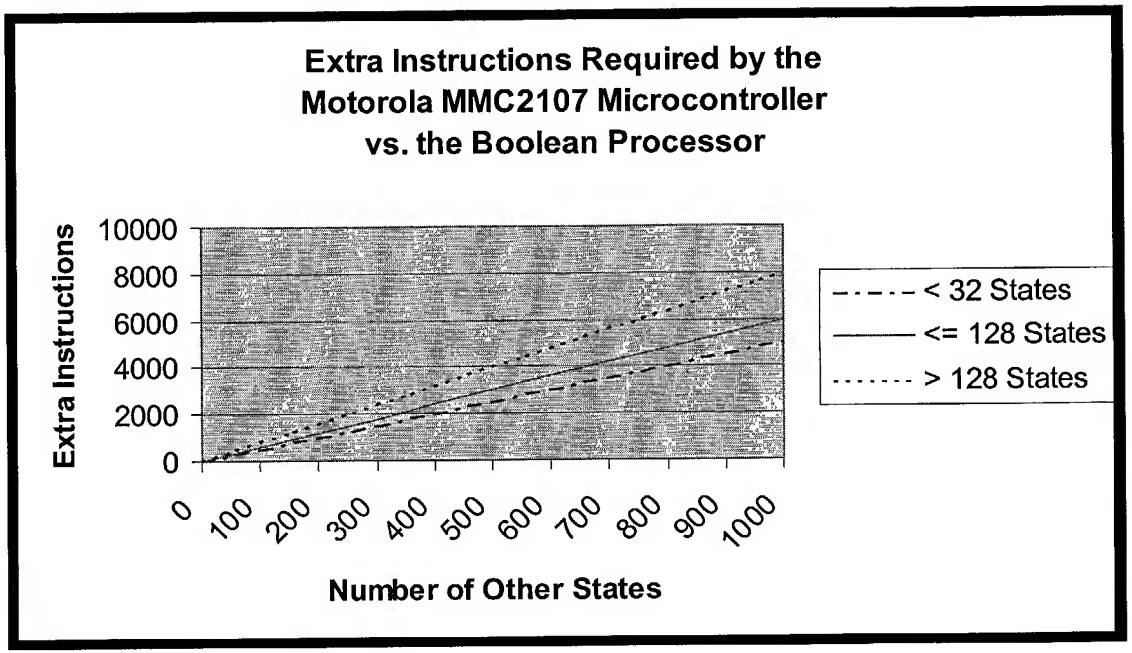
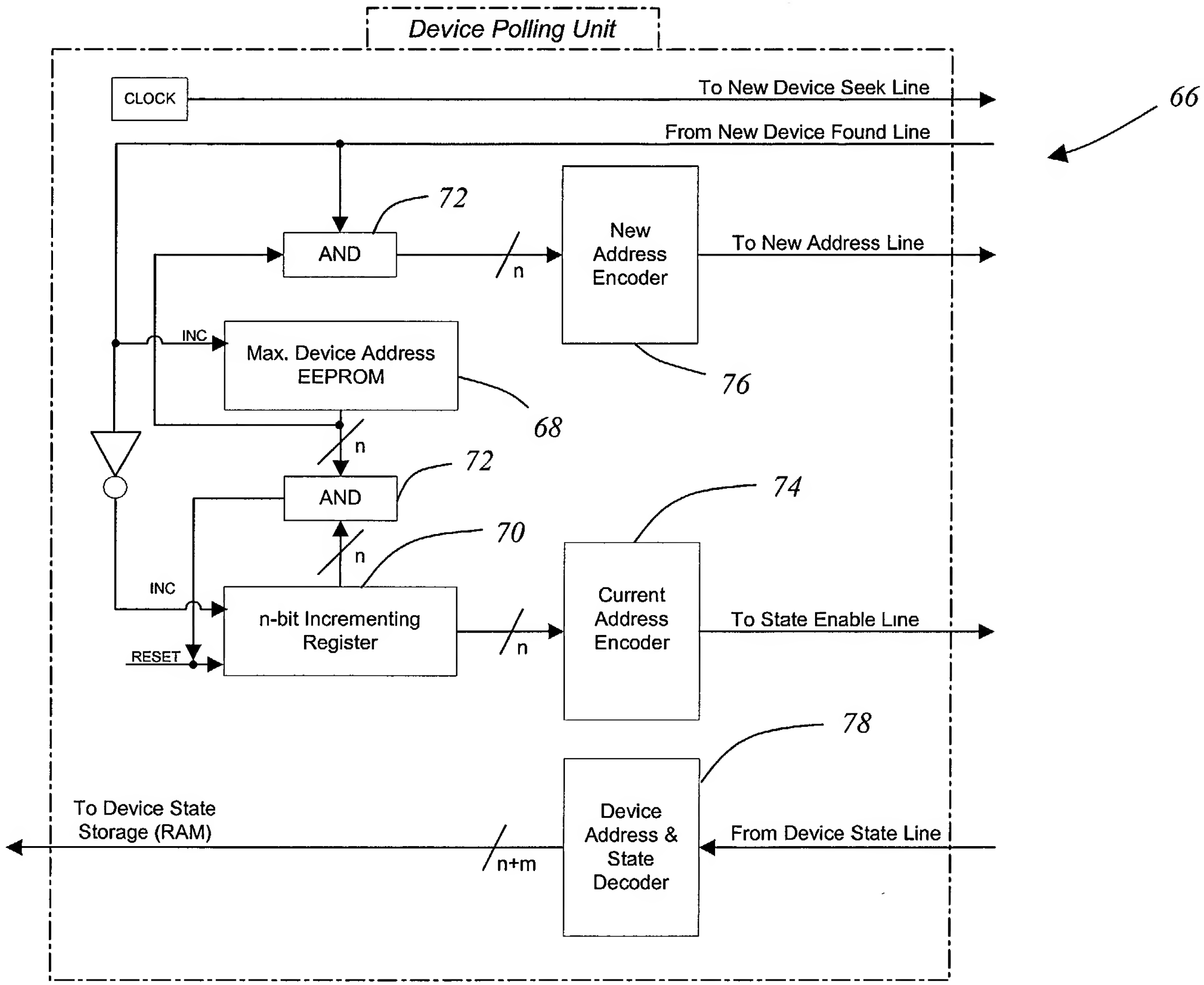

Extra Instructions Required by the
Motorola MMC2107 Microcontroller
vs. the Boolean Processor
Extra Instructions
10000
8000
6000
4000
2000
0
0
100
200
300
400
500
600
700
800
900
1000
Number of Other States
< 32 States
<= 128 States
> 128 States

Figure 17



Device Polling Unit
CLOCK
To New Device Seek Line
From New Device Found Line
66
72
AND
n
New
Address
Encoder
To New Address Line
INC
Max. Device Address
EEPROM
76
68
n
72
AND
74
70
n
INC
n-bit Incrementing
Register
RESET
n
Current
Address
Encoder
To State Enable Line
78
To Device State
Storage (RAM)
n+m
Device
Address &
State
Decoder
From Device State Line

Figure 18

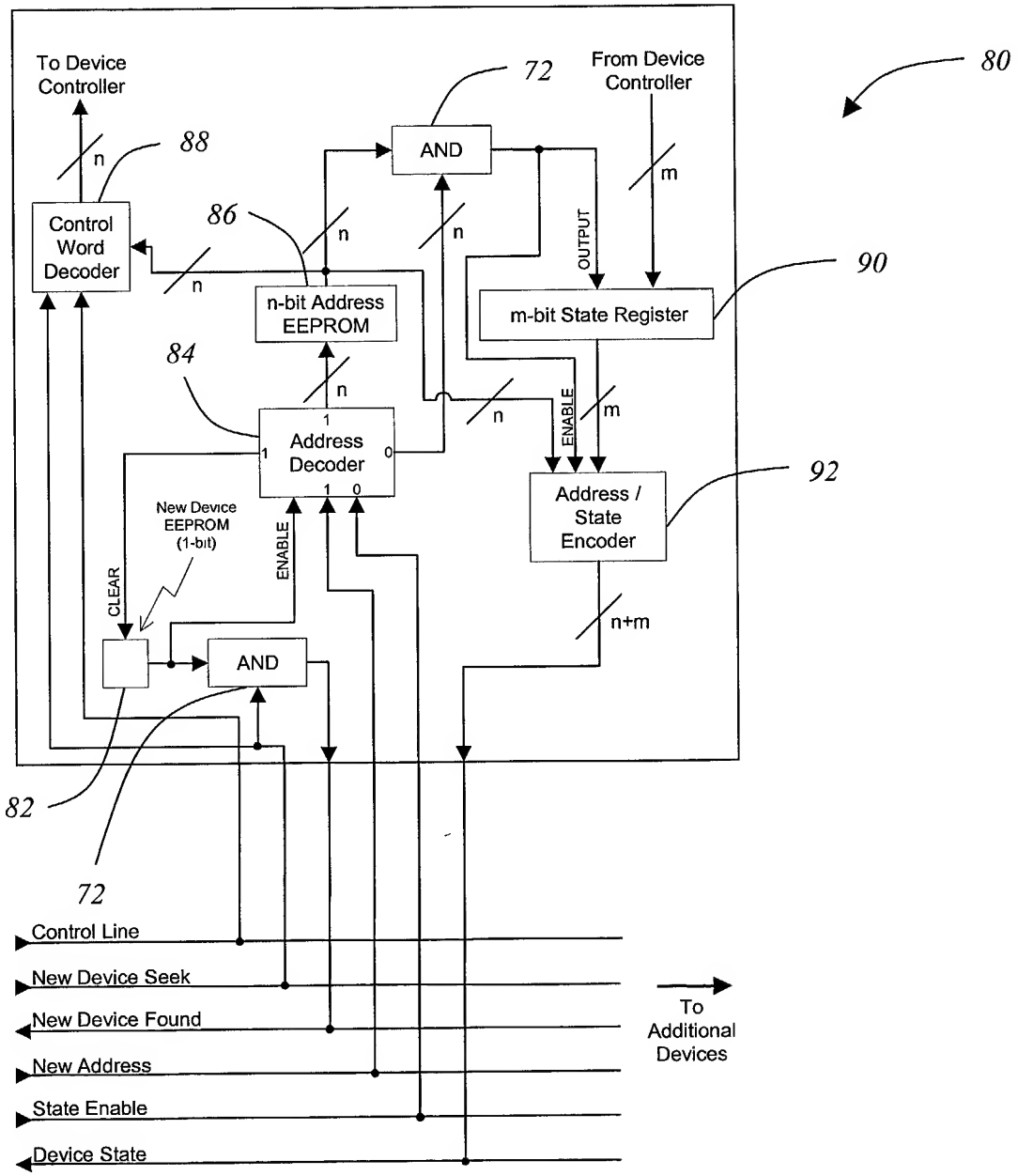


Figure 19

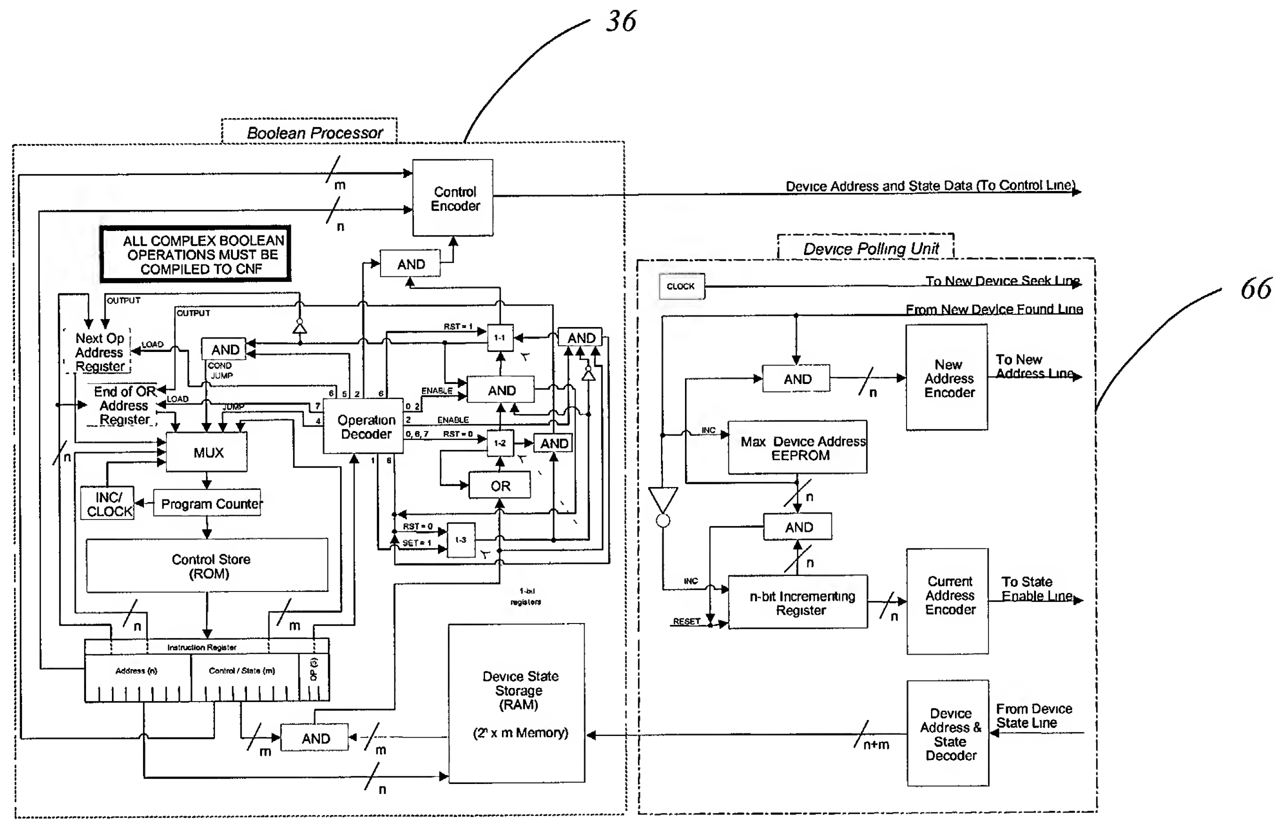

36
66
Boolean Processor
Control Encoder
Device Address and State Data (To Control Line)
ALL COMPLEX BOOLEAN OPERATIONS MUST BE COMPILED TO CNF
AND
Next Op Address Register
End of OR Address Register
MUX
INC/ CLOCK
Program Counter
Control Store (ROM)
Operation Decoder
OR
Instruction Register
Address (n)
Control / State (m)
Device State Storage (RAM) (2ⁿ x m Memory)
Device Polling Unit
CLOCK
To New Device Seek Line
From New Device Found Line
New Address Encoder
To New Address Line
Max Device Address EEPROM
n-bit Incrementing Register
Current Address Encoder
To State Enable Line
Device Address & State Decoder
From Device State Line
n+m

Figure 20

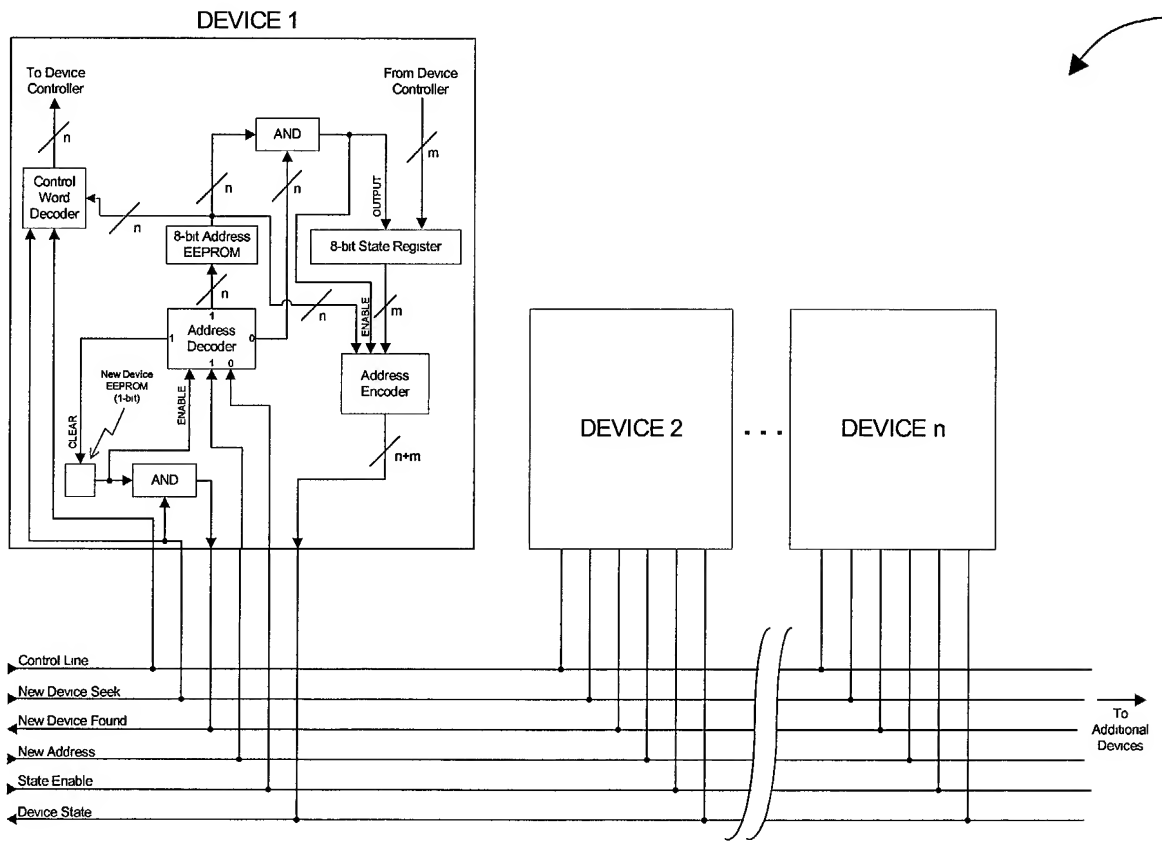

94
DEVICE 1
To Device Controller
From Device Controller
AND
n
m
Control Word Decoder
n
n
OUTPUT
8-bit Address EEPROM
8-bit State Register
n
Address Decoder
1
0
n
ENABLE
m
New Device EEPROM (1-bit)
ENABLE
CLEAR
Address Encoder
AND
n+m
DEVICE 2
DEVICE n
Control Line
New Device Seek
New Device Found
New Address
State Enable
Device State
To Additional Devices

Figure 21